ABSTRACT

A method of efficiently simulating logic designs comprising signals that are capable of having more than two unique decimal values and one or more unique drive states, such as designs based upon the new N-nary logic design style, is disclosed. The present invention includes a signal model that models N-nary signal value, drive strength, and signal definition information in a specific format that supports the ability of the simulator to simulate the operation of the N-nary logic gates such as adders, buffers, and multiplexers by arithmetically and logically manipulating the unique decimal values of the N-nary signals. The simulator comprises an input logic signal model reader, an arithmetic/logical operator, an output logic signal model generator, and an output message generator that generates one or more output- or input-signal-specific output messages that pack relevant simulation data into a format optimized to the architecture of the simulation host.